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Non-Destructive Contamination Detection in Thick and Extremely-Thin SOI Wafers Using Optical Second Harmonic Generation

FEMTOMETRIX Assuring Quality Interfaces

VANDERBILT UNIVERSITY

M.C. Kryger and J.P. Changala
FemtoMetrix, Inc., Santa Ana, California, USA

M. L. Alles
Vanderbilt University, Nashville, Tennessee, USA

Abstract

Non-destructive optical second harmonic generation (SHG) is shown to be an effective method for detecting surface and subsurface non-visual defects in commercial thick and extremely-thin (ET) SOI wafers. A method is demonstrated for removing contributions (noise) from layer thickness variations observed in thick SOI, increasing the sensitivity and enabling detection of trace surface metal contamination. Sub-surface contamination, otherwise missed by the standard flow of non-destructive characterization methods, is shown to be detected by SHG.

Fig. 1: Harmonic F1x® wafer inspection tool.

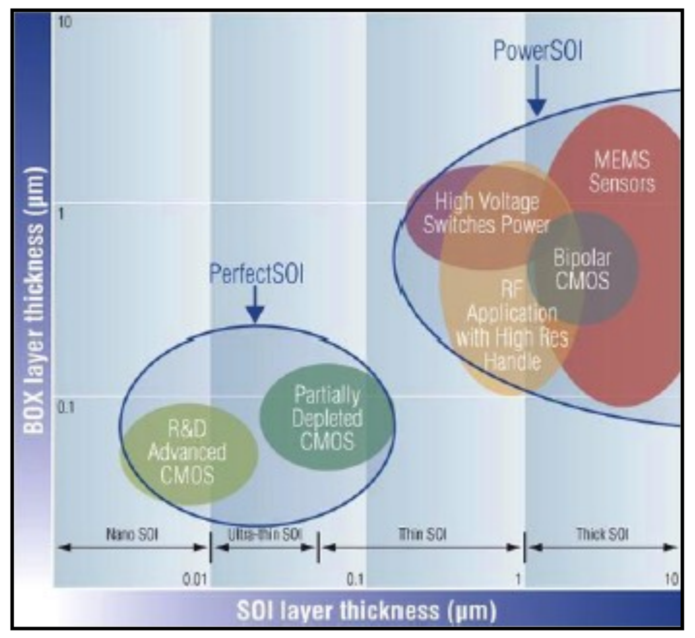

Fig. 2: An example of SOI types and applications from SunEdison Semi, a major manufacturer of SOI wafers, PerfectSOI = thin and PowerSOI = thick.

Background

Optical Second Harmonic Generation (SHG) is a nondestructive, contactless technique for characterizing surfaces, interfaces, thin-films and bulk properties of materials. SHG originates from areas where symmetry in the material is broken, such as surfaces, interfaces, crystal defects, and the bulk of non-centrosymmetric materials. This allows SHG to be highly interface specific in centrosymmetric materials like silicon and Silicon-on-Insulator (SOI), and effectively probe the bulk of materials such as Ge and III-V. Novel layered materials necessary to continue meeting the exacting performance needs of device fabricators, such as SOI, are excellent candidates for characterization with SHG [1-5].

A significant plurality of reliability, yield, and variability concerns in SOI are due to charge traps and associated defects at the Device/BOX and BOX/Bulk interfaces [2,3]. Charge traps in the near-interfacial regions of the BOX layer in FD-SOI substrates (Dit) can lead to significant bias temperature instabilities, especially in fully-depleted transistors [2,4]. Hot carrier stress due to trapping at the back gate is also known to have detrimental impact on FD-SOI transistor reliability [5]. Other key yield concerns such as 1/f - or "flicker" - noise are additionally attributable to Dit complications [6]. One source of excessive charge traps is buried trace metal contamination [7]. The effect of metal contamination may also be compounded during production by the failure of traditional metal gettering techniques in FD-SOI [8]. In addition, normal methods of monitoring metal contamination in bulk silicon are not effective for FD-SOI [9], resulting in defective wafers being processed as seen in Figure 3 below.

Wafer Path	In-line Analysis	Destructive Test	Goes to Production
Good wafer not selected for random destructive test	✓	N/A	✓
Good wafer selected for random destructive test	✓	✓	✗
Surface defective wafer	✗	✗	✗
Contaminated wafer not selected for random destructive test	✓	N/A	✓
Contaminated wafer selected for random destructive test	✓	✗	✗

Fig. 3: Wafer fabrication path.

TOOL USES	1 VPD-ICPMS + SIMS / GD-OES	2 ψ-MOS + DLTS	3 TXRF + X-Ray	2nd Harmonic Generation: Harmonic F1x®
Structural Defects	✗	✓	✗	✓
Non-Destructive	✗	✗	✓	✓
Throughput + NVD Sensitivity	✗	✗	✗	✓
Device / BOX Interface	✓	✓	✗	✓
Bulk / BOX Interface	✓	✗	✗	✓

Fig. 4: Comparison of metrology techniques.

Cu is considered more dangerous than iron due to its diffusive properties, and when located on the backside of an SOI wafer can easily penetrate into the BOX during standard processing. Once Cu is introduced into the buried interfaces of an SOI wafer it will diffuse throughout the wafer [10]. The extremely thin layers employed by FD-SOI introduce new metrology challenges requiring characterization of the electrical parameters of BOX interfaces where conventional techniques have limitations [11]. Figure 4 summarizes in-line and subsurface capabilities of relevant characterization tools.

SHG is a non-destructive, contactless technique for characterizing surfaces, interfaces, thin-films and bulk properties of materials. SHG is the only non-destructive in-line method able to comprehensively characterize the quality of BOX interfaces in FD-SOI substrates, due to its high throughput and high sensitivity to disturbances in the electric field at the interfaces of multilayered materials [12,13]. As an industrial tool, SHG offers distinct yield and net cost advantages.

Procedure

Eight SOI wafers, comprising two sets of four, were provided by a leading semiconductor industry firm for the evaluation of the Harmonic F1x®. Each set of four contained a distinct type of SOI, thick (1500/1000 nm) and thin (12/25 nm.)

The four thick film 200 mm SOI wafers were intentionally contaminated with Cu to study the sensitivity of SHG to surface contamination. All four of the wafers were measured nondestructively (SHG, Spectroscopic Reflectometry) and destructively (VPD-ICPMS). One wafer was held as a control and not intentionally contaminated. The remaining three were spincoat with Cu in doses on the orders of 10^{10}, 10^{11}, and 10^{12} at/cm^2.

The four thin film 300 mm SOI wafers were measured via SHG as delivered to inspect for non-visual defects that influence yield. Of the four thin wafers there were two pairs of two, each having a distinct manufacturing process. These wafers were measured non-destructively (SHG, Spectroscopic Ellipsometry, Surfscan), and destructively (VPD-ICPMS, LA-ICPMS).

Results

Initial results from the three intentionally contaminated 1500/1000 nm SOI samples did not indicate a stark contrast versus control as expected. Within wafer variation was high, and there was not an obvious relationship between Cu dose and SHG signal. Figure 6 below shows the initial (raw data) SHG response maps from the four wafers.

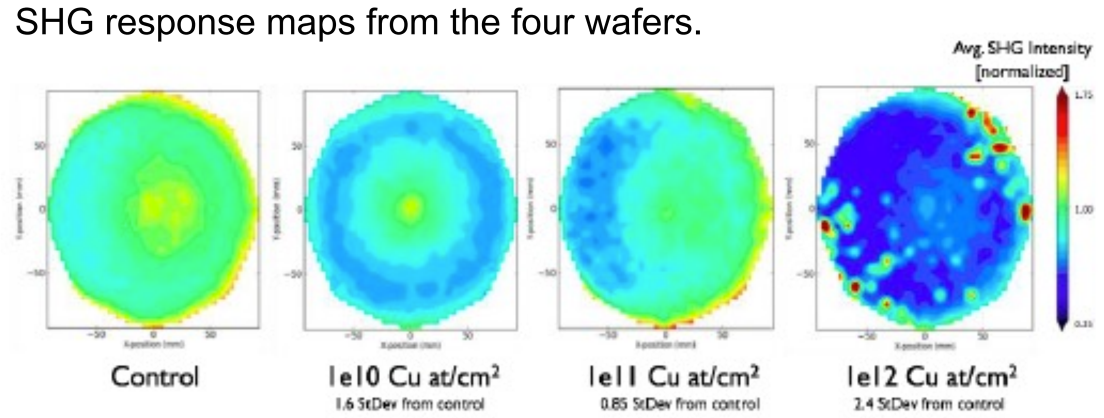

Figure 7: SHG maps of 1500/1000 nm SOI.

	Control wafer	10^{10}	10^{11}	10^{12}
Wafer Average response (normalized to control)	1.0	0.79	0.89	0.69
Minimum response	0.79	0.66	0.58	0.43
Maximum response	1.47	1.18	1.74	3.42
StDev	0.13	0.09	0.17	0.31
# of StDevs wafer average from control	0	1.6	0.85	2.4

Table 1: SHG results from 1500/1000 nm SOI.

The large overlap in signal levels from the different Cu concentrations is more clearly seen above in Table 1. From the results in Figure 7 and in Table 1, there is trending behavior in the overall SHG response based on the copper contamination, but it is highly obscured by the within-wafer variation. This suggests some other variable that is making it difficult to draw a clear correlation between the simple SHG parameter and Cu contamination. To more fully characterize the thick film wafer set, Spectroscopic Reflectometry (SR) was performed to generate layer thickness maps, shown in Figure 8.

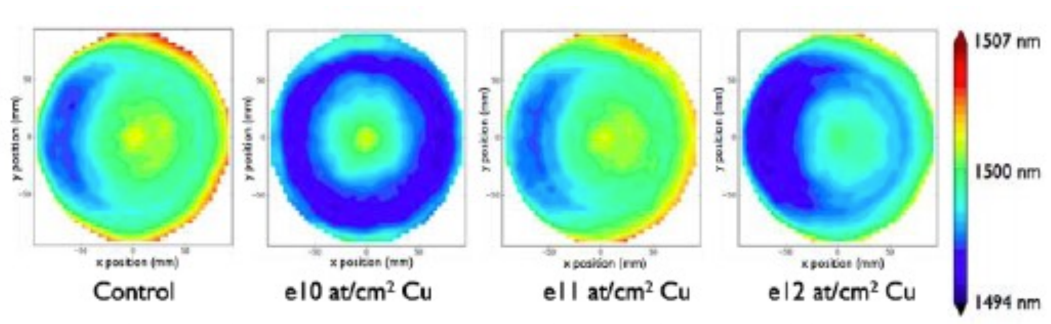

Fig. 8: SR Top Si Film Thickness Maps for 1500/1000 nm SOI.

This systematic similarity led to exploration of layer thickness parsing as a means of improving sensitivity to metallic contamination and other electrically active contributions to the SHG signal.

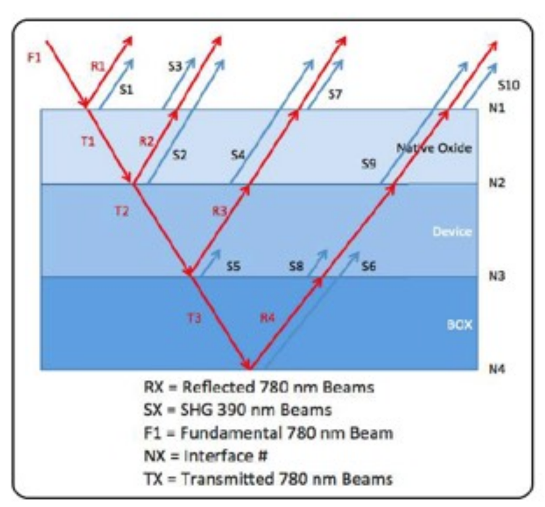

Fig. 9: Fundamental and SHG beam paths within the 1500/1000 nm SOI structure.

To illustrate the layer thickness effects a diagram of the SOI structure listing the potential fundamental and SHG beam paths is shown in Figure 9. The fundamental beam passing through the top silicon film (T2 and T3) would reflect (R3 and R4) off the buried interfaces (N3 and N4), and travel back up through the top Si film without complete absorption. This reflected beam, when reaching the top interfaces (N1 and N2), causes interference effects with the incoming fundamental light, thus affecting the SHG signal. By removing these "background noise" components, the sensitivity is increased, allowing probing of the electrically active properties of the material under test.

With the film thickness variation effects parsed from the SHG signal, the remaining variations in SHG response can be primarily attributed to electrically active parameters.

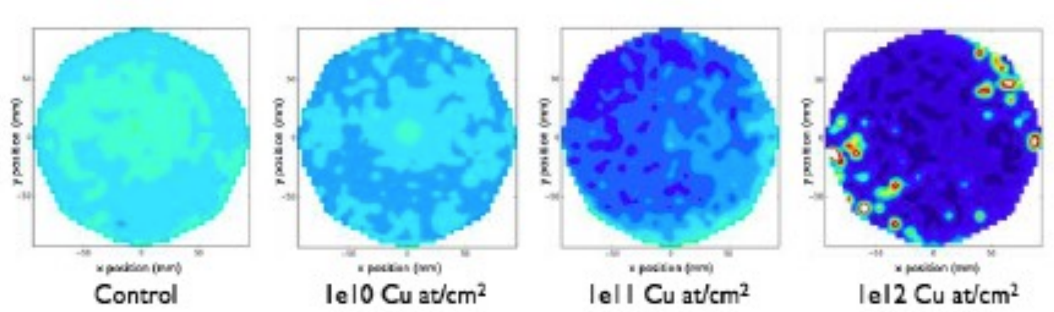

Fig. 10: SHG maps of 1500/1000 nm SOI wafers after parsing layer thickness.

Results Continued

The four thin film SOI wafers from the two batches did not have defectivity outside of specification per spectroscopic ellipsometry or Surfscan characterization (Table 2, Figure 11). The destructive VPD-ICPMS characterization on each twin wafer indicated that the wafers tested were within ITRS 2016 spec for Cu contamination [14]. All correlative results indicated no production challenge for any tested sample: all four wafers would have been used for device fabrication had they not been randomly selected for this study.

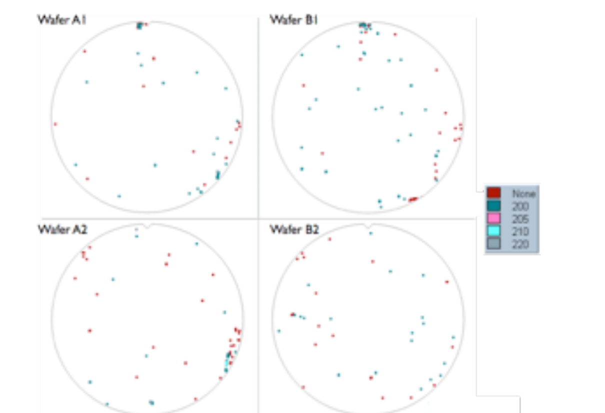

Figure 11: Surfscan surface defect results on 12/25 nm SOI.

Wafer	Manufacturing Process	Characterization Techniques	VPD ICPMS Cu Results [Atom/cm²]	SHG Testing	SE Mean Device / BOX Thickness
A1	A	S.Ellipsometry, Surfscan	N/A	Yes	12.6 nm / 25.2 nm
A2	A	(...) + VPD-ICPMS	2E+7	No	12.7 nm / 25.1 nm
B1	B	S.Ellipsometry, Surfscan	N/A	Yes	12.2 nm / 25.1 nm
B2	B	(...) + VPD-ICPMS	4E+7	No	12.3 nm / 25.1 nm

Table 2: Characterization techniques / results on 12/25 nm SOI.

The normalized SHG data from wafers A1 and B1 shows the SHG signal deviating from a baseline average value of 1. The mean SHG response of each wafer was chosen as the basis for normalization as the VPD-ICPMS data from the twin wafers suggested average metal contamination well within ITRS specification [14]. Maps of these normalized results are shown in Figure 12.

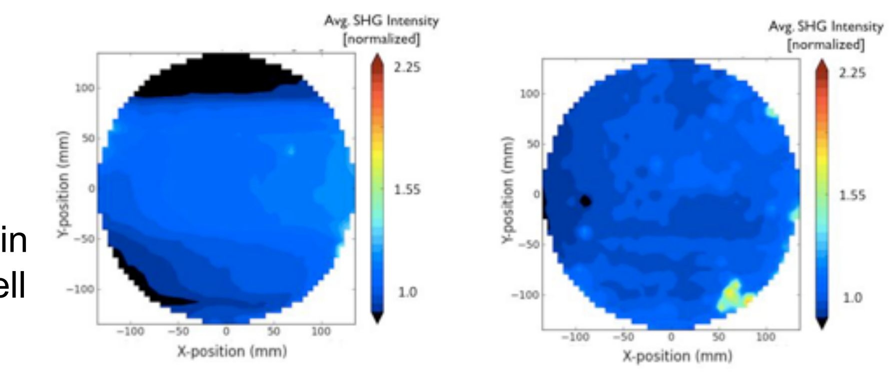

Fig. 12: Normalized SHG maps of wafers A1 and B1.

On wafer A1 the within wafer SHG variation remains within three standard deviations of the wafer mean SHG response, while wafer B1 follows this variation trend of remaining within a three standard deviation band with the exception of a few areas along the edge of the wafer. As seen on wafer B1 in Figure 13, three areas exceeded the three standard deviation band. The largest of these areas of increased signal exceeded the baseline by more than 12 standard deviations, indicating presence of a non-visual defect, as complementary optical mapping of the wafer using the Surfscan technique did not indicate production relevant surface concern where anomalous SHG signal was present (spot 3 on Figure 13). The region with highest anomalous signal (spot 3) alongside a control from within baseline was cleaved and sent to a third party lab for elemental composition testing by laser ablation ICP mass spectrometry (LA ICP-MS). Results were 3.5e10^{11} at/cm^2 concentration of Cu on spot 3 and no detectable Cu on the within-baseline control.

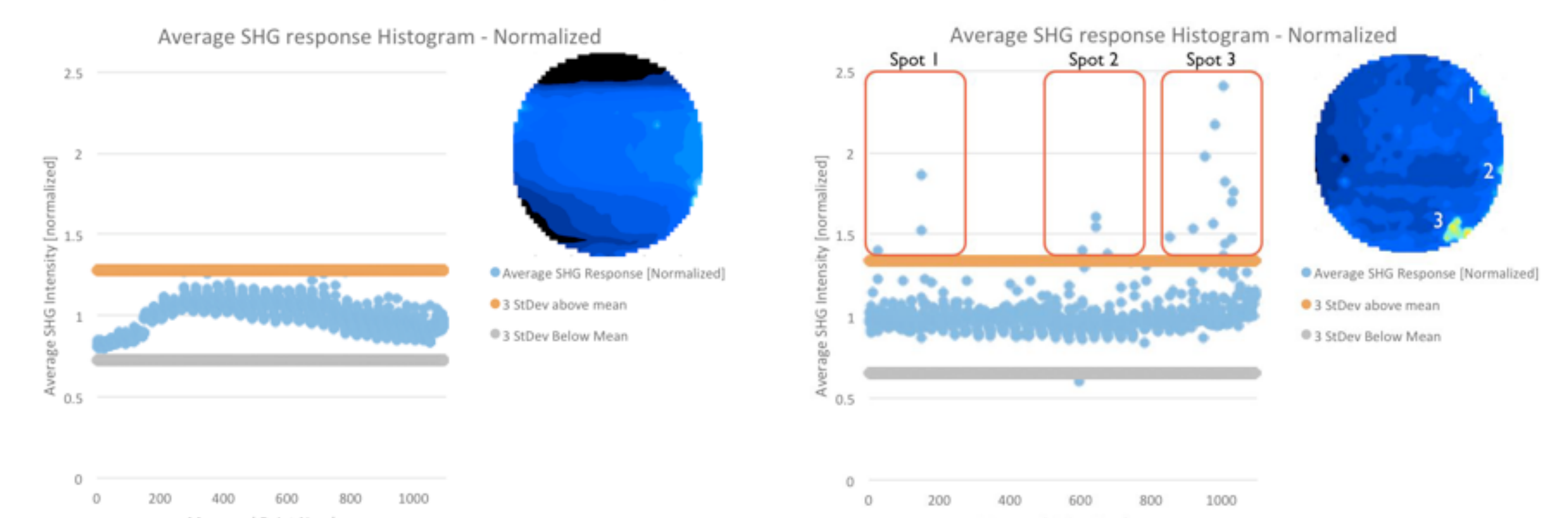

Fig. 13: Statistical bands on wafer A1 and B1 showing areas with up to 12.4 standard deviations from baseline on B1.

Of the four thin wafers characterized and presumed production worthy, one was contaminated with sub-surface Cu. SHG demonstrated efficacy in characterization of the non-visual defect missed by other techniques, which would likely have induced yield excursion, confirmed by LA-ICPMS.

Thus while ET SOI offers performance and cost advantages for sub-30nm CMOS, and thick SOI enables many power, high voltage, and RF applications [15,16,17], cost-effective production can be complicated by yield excursions and reliability concerns resulting from an inability to adequately characterize buried interfaces for high volume manufacturing purposes. As evidenced by the thin SOI SHG results versus other characterization efforts, SHG was demonstrated as a means to characterize non-visual defect that other in-line non-destructive techniques could not. Therefore by using SHG alongside other in-line optical characterization techniques the use of destructive techniques can be reduced via effective targeting, enabling increased efficiency, reduced waste and enhanced yield.

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